



SPECIFICATION FOR LCM Module

MODULE No:	KD035QHFID161
CUSTOMER:	

STARTEK	INITIAL	DATE
PREPARED BY	Distributed by:  www.texim-europe.com	
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常备库存 Stock For Sale	长期供货 Long Time supply	支持小量 NO MOQ	品种齐全 In Full Range	

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* Descriptions

This is a color active matrix TFT (Thin Film Transistor) LCD (liquid crystal display) that uses amorphous silicon TFT as a switching device. This module is composed of a Transmissive type TFT-LCD Panel, driver circuit, back-light unit. The resolution of a 3.54 " TFT-LCD contains 640x960 pixels, and can display up to 16.7M colors.

* Features

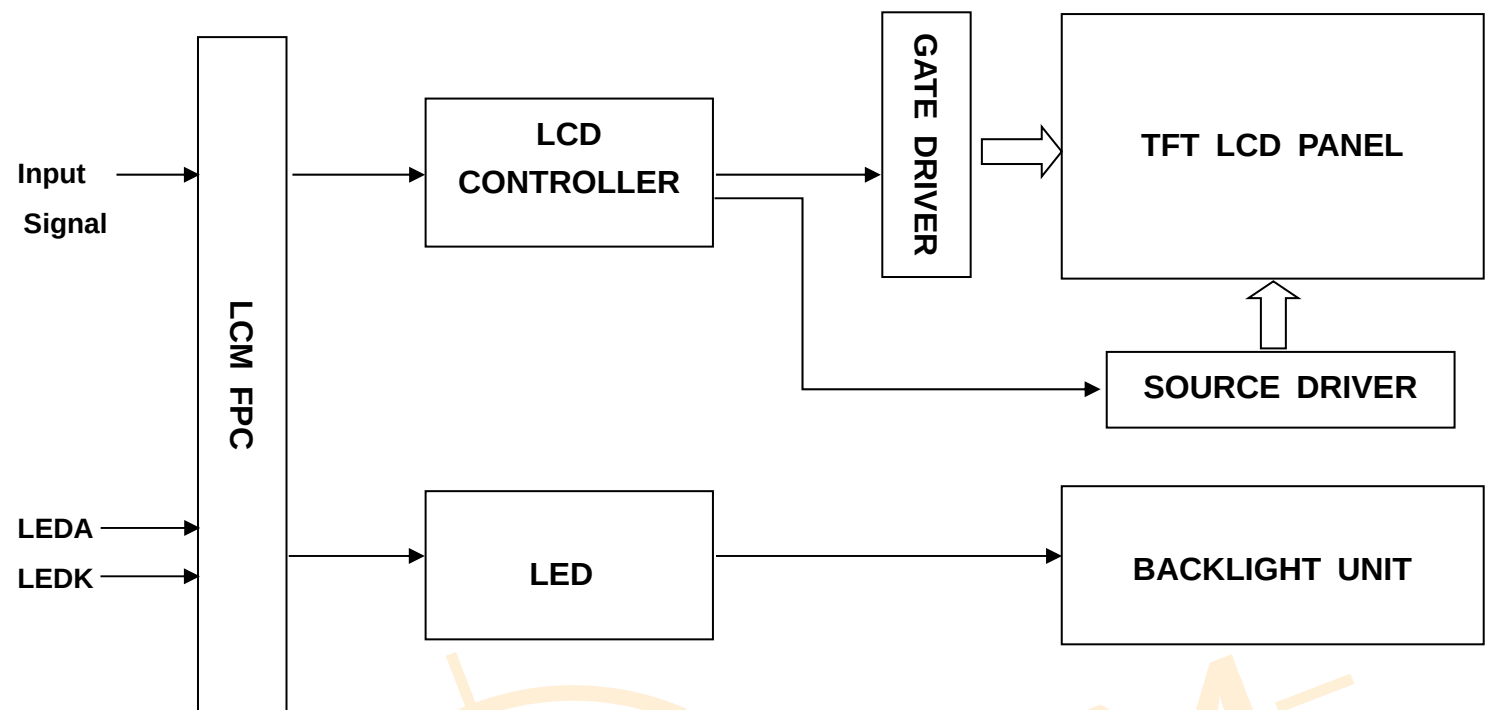
General Information Items	Specification	Unit	Note
	Main Panel		
Display area(AA)	49.92(H)*74.88(V) (3.54 inch)	mm	
Driver element	TFT active matrix	-	
Display colors	65K/262K/16.7M	colors	
Number of pixels	640(RGB)*960	dots	
Pixel arrangement	RGB vertical stripe	-	
Pixel pitch	0.078(H)*0.078(V)	mm	
Viewing angle	Free	o'clock	
Controller IC	ST7703	-	
LCM Interface	4Lane MIPI	-	
Display mode	Transmissive /Normally Black	-	
Operating temperature	-30~+85	℃	
Storage temperature	-30~+85	℃	

* Mechanical Information

Item		Min.	Typ.	Max.	Unit	Note
Module size	Horizontal(H)	-	54.98	-	mm	Without hook
	Vertical(V)	-	84.42	-	mm	Without hook
	Depth(D)	-	2.55	-	mm	
Weight		-	25	-	g	

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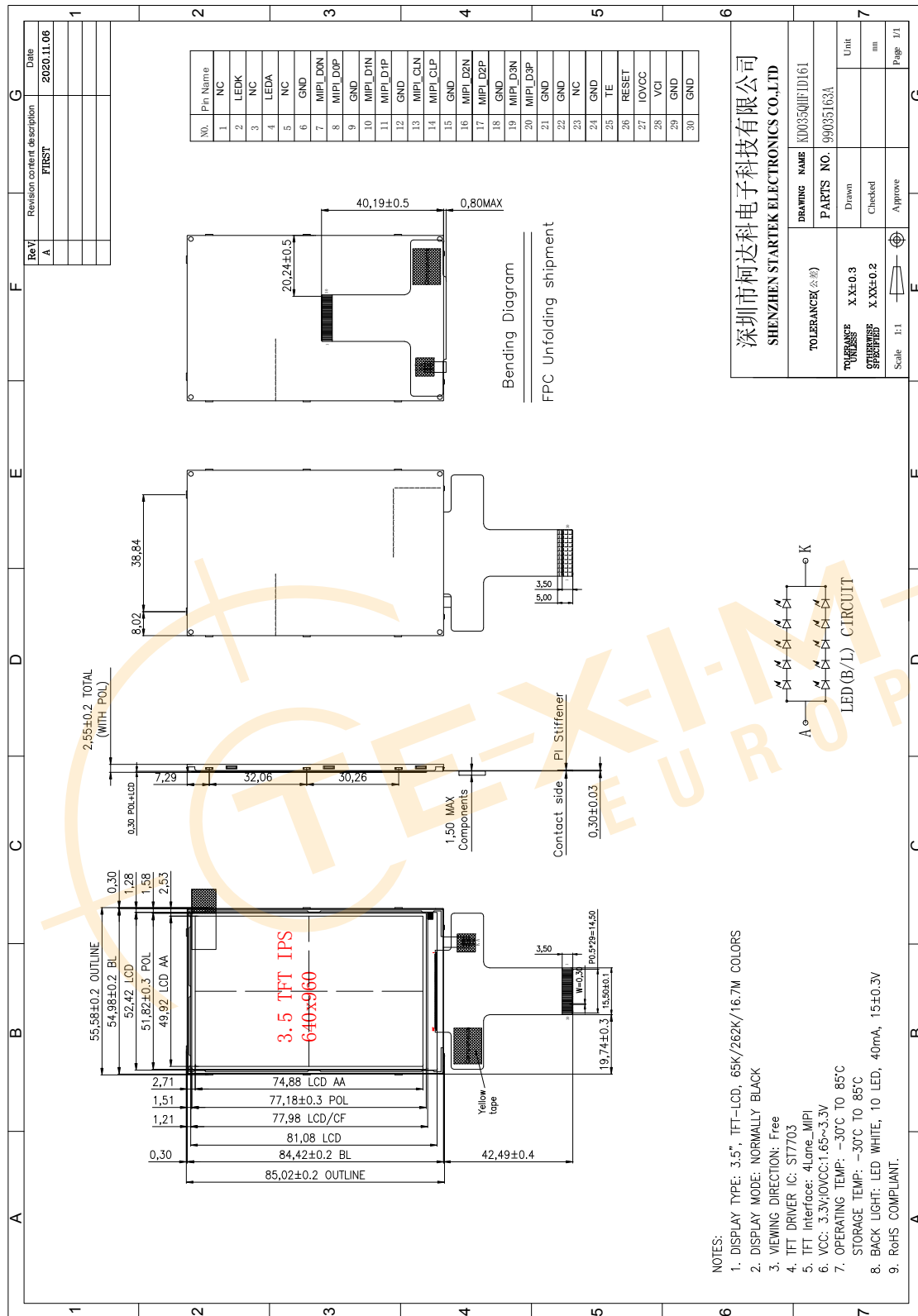
1. Block Diagram



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2. Outline dimension



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Long Time supply

支持小量
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3. Input terminal Pin Assignment

NO.	SYMBOL	DISCRIPTION	I/O
1	NC	--	--
2	LEDK	Cathode pin of backlight.	P
3	NC	--	--
4	LEDA	Anode pin of backlight.	P
5	NC	--	--
6	GND	Ground.	P
7	MIPI_D0N	- MIPI DSI differential data pair. (Data lane 0)	I
8	MIPI_D0P		I
9	GND	Ground.	P
10	MIPI_D1N	- MIPI DSI differential data pair. (Data lane 1)	I
11	MIPI_D1P		I
12	GND	Ground.	P
13	MIPI_CLN	- MIPI DSI differential clock pair	I
14	MIPI_CLP		I
15	GND	Ground.	P
16	MIPI_D2N	- MIPI DSI differential data pair. (Data lane 2) Leave it o to GND level when not in use.	I
17	MIPI_D2P		I
18	GND	Ground.	P
19	MIPI_D3N	- MIPI DSI differential data pair. (Data lane 3) Leave it to GND level when not in use.	I
20	MIPI_D3P		I
21	GND	Ground.	P
22	GND	Ground.	P
23	NC	--	--
24	GND	Ground.	P
25	TE	- Tearing effect output pin. Leave the pin open when not in use.	O



26	RESET	- The external reset input Initializes the chip with a low input. Be sure to execute a power-on reset after supplying power.	I
27	IOVCC	I/O power supply voltage.	P
28	VCI	Supply Voltage .	P
29	GND	Ground.	P
30	GND	Ground.	P



4. LCD Optical Characteristics

4.1 Optical specification

Item		Symbol	Condition	Min.	Typ.	Max.	Unit.	Note
Contrast Ratio		CR	$\Theta=0$ Normal viewing angle	800	1000	--		(1)(2)
Response time	Rising	T_R+T_F		--	35	40	msec	*(1)(3)
	Falling							
Color Gamut		S(%)		65	70	--	%	
Color Filter Chromaticity	White	W_X		0.2440	0.2840	0.3240		(1)(4) CA-310
		W_Y		0.2830	0.3230	0.3630		
	Red	R_X		0.5935	0.6335	0.6735		
		R_Y		0.3035	0.3435	0.3835		
	Green	G_X		0.2550	0.2950	0.3350		
		G_Y		0.5345	0.5745	0.6145		
	Blue	B_X		0.1045	0.1445	0.1845		
		B_Y		0.0273	0.0673	0.1073		
Viewing angle	Hor.	Θ_L	CR>10	--	85	--	*(1)(4)	
		Θ_R		--	85	--		
	Ver.	Θ_U		--	85	--		
		Θ_D		--	85	--		
Option View Direction		Free						

Measuring Condition

Measuring surrounding : dark room

Ambient temperature : $25 \pm 2^\circ\text{C}$

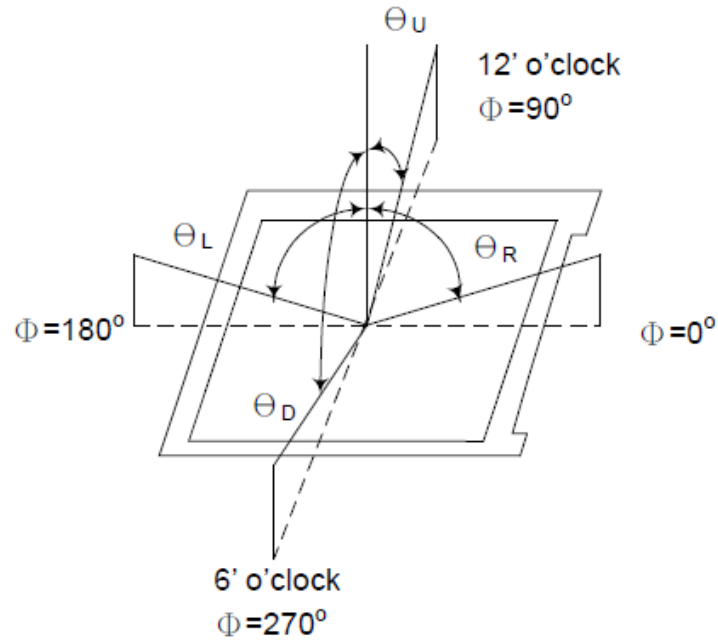
15min. warm-up time.

Measuring Equipment

FPM520 of Westar Display technologies, INC., which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics.

Note (1): Definition of Viewing Angle :

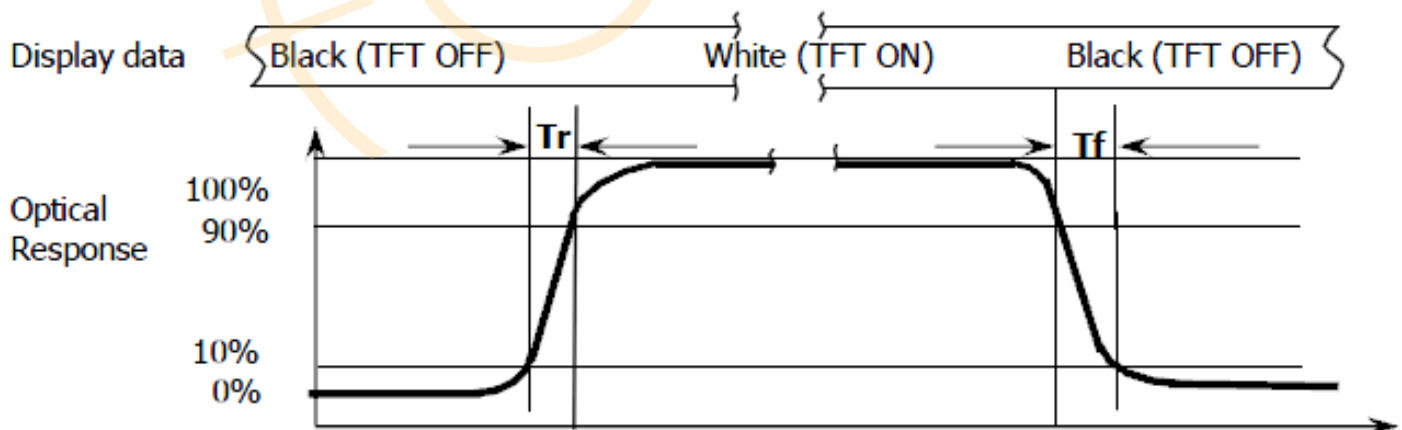
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Note (2): Definition of Contrast Ratio(CR) :measured at the center point of panel

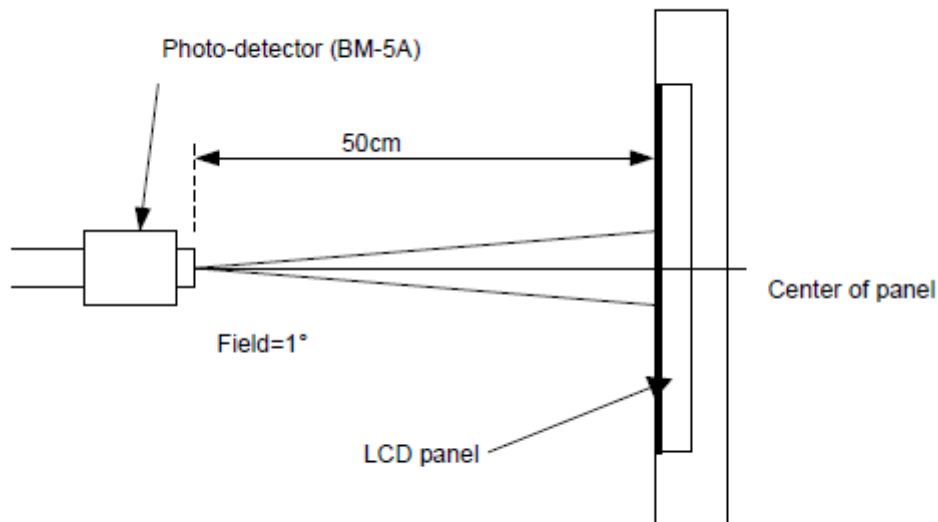
$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

Note (3): Response Time



Note (4): Definition of optical measurement setup

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5. Electrical Characteristics

5.1 Absolute Maximum Rating

Characteristics	Symbol	Min.	Max.	Unit	Note
Digital Supply Voltage	V _{CI}	-0.3	+6.6	V	Note1
Digital interface supply Voltage	IOVCC	-0.3	+5.5	V	Note1
Operating temperature	T _{OP}	-30	+80	°C	
Storage temperature	T _{ST}	-30	+85	°C	

NOTE1: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

5.2 DC Electrical Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Note
Digital Supply Voltage	V _{CI}	2.5	3.3	3.8	V	
Digital interface supply Voltage	IOVCC	1.65	1.8	2.0	V	
Normal mode Current consumption	I _{VCI}	--	50	60	mA	
Level input voltage	V _{IH}	0.7*IOVCC	--	IOVCC	V	
	V _{IL}	GND	--	0.3*IOVCC	V	
Level output voltage	V _{OH}	0.8*IOVCC	--	IOVCC	V	
	V _{OL}	GND	--	0.2*IOVCC	V	

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5.3 LED Backlight Characteristics

The back-light system is edge-lighting type with 10 chips LED

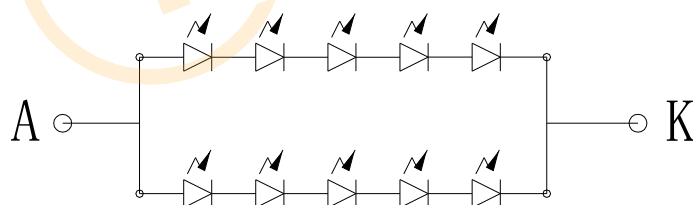
Item	Symbol	Min.	Typ.	Max.	Unit	Note
Forward Current	I_F	35	40	--	mA	
Forward Voltage	V_F	--	15	--	V	
LCM Luminance	LV	450	500	--	cd/m ²	Note3
LED life time	Hr	--	50000	--	Hour	Note1,2
Uniformity	Avg	80	--	--	%	Note3

Note1: LED life time (Hr) can be defined as the time in which it continues to operate under the condition:

$T_a = 25 \pm 3^\circ\text{C}$, typical IL value indicated in the above table until the brightness becomes less than 50%.

Note 2: The "LED life time" is defined as the module brightness decrease to 50% original brightness at

$T_a = 25^\circ\text{C}$ and $I_L = 40\text{mA}$. The LED lifetime could be decreased if operating I_L is larger than 40mA. The constant current driving method is suggested.

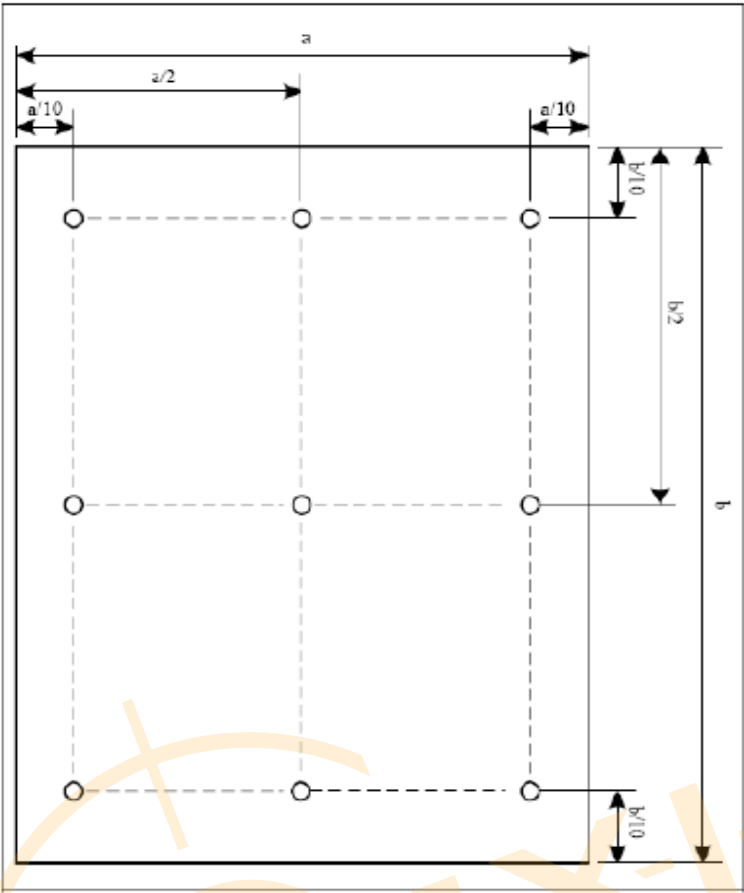


LED (B/L) CIRCUIT

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Note (3) Luminance Uniformity of these 9 points is defined as below:



$$\text{Uniformity} = \frac{\text{minimum luminance in 9 points (1-9)}}{\text{maximum luminance in 9 points (1-9)}}$$

$$\text{Luminance} = \frac{\text{Total Luminance of 9 points}}{9}$$

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5.4 DSI DC Characteristics

LP Mode

Parameter	Symbol	Conditions	Spec.			Unit
			Min.	Typ.	Max.	
Logic high level input voltage	V_{IHLPCD}	LP-CD	450	-	1350	mV
Logic low level input voltage	V_{ILLPCD}	LP-CD	0	-	200	mV
Logic high level input voltage	V_{IHLPRX}	LP-RX(CLK, D0)	880	-	1350	mV
Logic low level input voltage	V_{ILLPRX}	LP-RX(CLK, D0)	0	-	550	mV
Logic low level input voltage	$V_{ILLPRXULP}$	LP-RX(CLK ULP mode)	0	-	300	mV
Logic high level output voltage	V_{OHLPTX}	LP-TX(D0)	1.1	-	1.3	V
Logic low level output voltage	V_{OLLPTX}	LP-TX(D0)	-50	-	50	mV
Logic high level input current	V_{IH}	LP-CD, LP-RX	-	-	10	uA
Logic low level input current	V_{IL}	LP-CD, LP-RX	-10	-	-	uA
Input pulse rejection	SGD	DSI-CLK+/-, DSI-D0+/-1	-	-	300	Vps

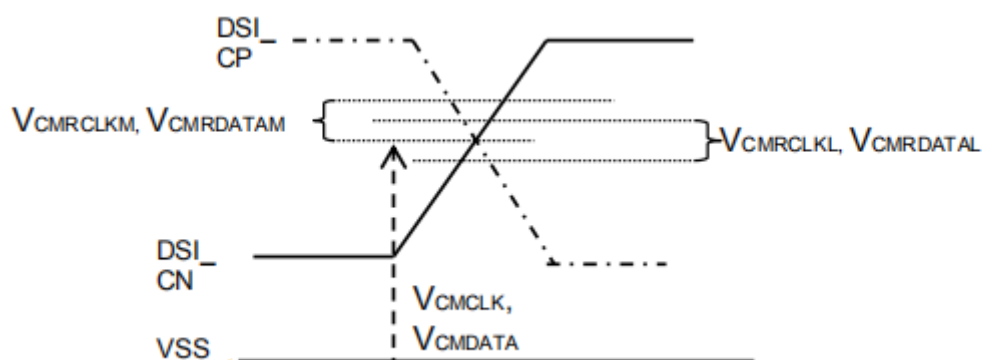


*Input glitch rejections of low-power receivers

High Speed Mode

Parameter	Symbol	Conditions	Spec.			Unit
			Min.	Typ.	Max.	
Input common mode	V_{CMCLK} V_{CMDATA}	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	70	-	330	mV
Input common mode variation <450 MHz	$V_{CMRCLKL}$ $V_{CMRDATAL}$	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-50	-	50	mV
Input common mode variation >450 MHz	$V_{CMRCLKM}$ $V_{CMRDATAM}$	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-	-	100	mV
Low-level differential Input threshold	V_{THLCLK} $V_{THLDATA}$	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-70	-	-	mV
High-level differential Input threshold	V_{THHCLK} $V_{THHDATA}$	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-	-	70	mV
Single ended input low voltage	V_{ILHS}	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-40	-	-	mV
Single ended input high voltage	V_{IHHS}	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-	-	460	mV
Differential input termination resistor	R_{TERM}	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	80	100	125	Ω
Single-ended threshold voltage for termination enable	V_{TERMEN}	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-	-	450	mV
Termination capacitor	C_{TERM}	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-	-	-	pF

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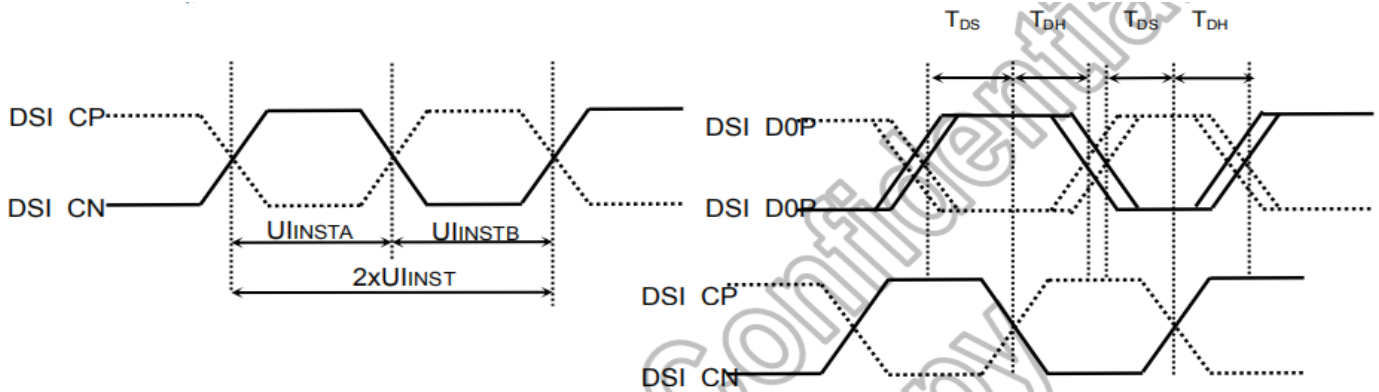
*Differential voltage range and Command mode voltage

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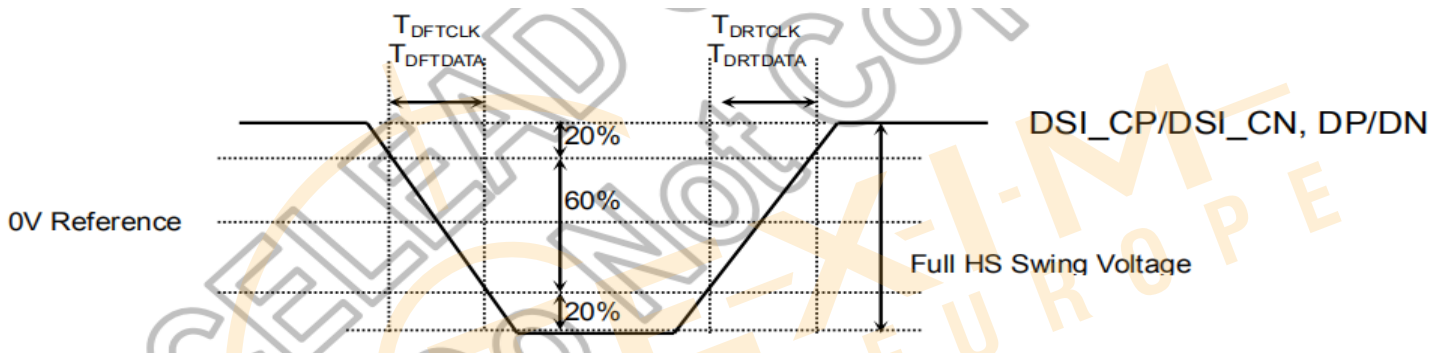
6. AC Characteristics

6.1 DSI Interface Timing Characteristics:

6.1.1 High Speed Mode



***DSI clock timing Characteristics**



***Rising and falling time on clock and data channel**

(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.5V to 3.3V, TA = -30 to 70°C)

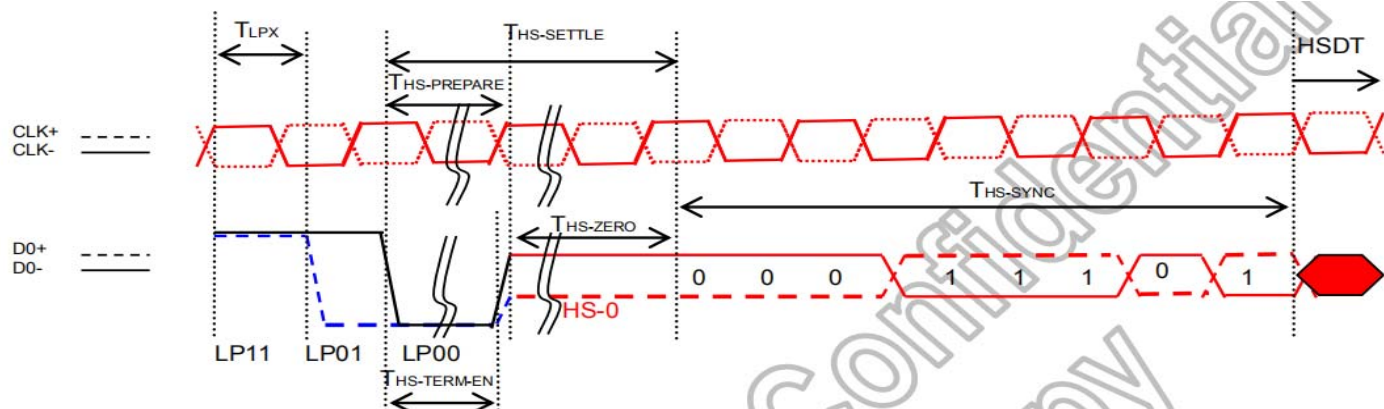
Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_CP/ DSI_CN	Double UI instantaneous	2xUIINST	TBD	-	25	ns
	UI instantaneous	UIINSTA UIINSTB	TBD	-	12.5	ns
DP/DN	Data to clock setup time	T _{DS}	0.15xUI	-	-	ps
	Data to clock hold time	T _{DH}	0.15xUI	-	-	ps
DSI_CP/ DSI_CN	Differential rise time for clock	T _{DRTCLK}	150	-	0.3UI	ps
	Differential fall time for clock	T _{DFTCLK}	150	-	0.3UI	ps
DP/DN	Differential rise time for data	T _{DRTDATA}	150	-	0.3UI	ps
	Differential fall time for data	T _{DFTDATA}	150	-	0.3UI	ps

***DSI High Speed Mode Characteristics**

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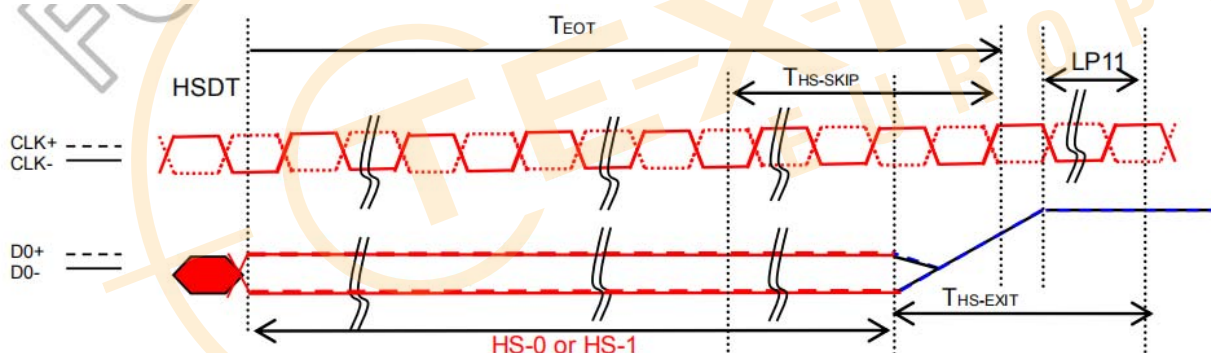
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6.1.3 Bursts Mode



Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_D0P/ DSI_D0P	Length of LP-00/LP01/LP10/LP11	T _{LPX}	50	-	-	ns
	Time to Driver LP-00 to prepare for HS transmission	T _{HS-PREPARE}	40+4UI	-	85+6UI	ns
	Time to enable data receiver line termination	T _{HS-TERM-EN}	-	-	35+4xUI	ns
	Time to drive LP-00 by display module	T _{TA-GET}	5xT _{LPXD}	-	-	ns
	Time to drive LP-00 after turnaround request Host	T _{TAGO}	4xT _{LPXD}	-	-	ns

*DSI Low Power Mode to High Speed Mode Timing



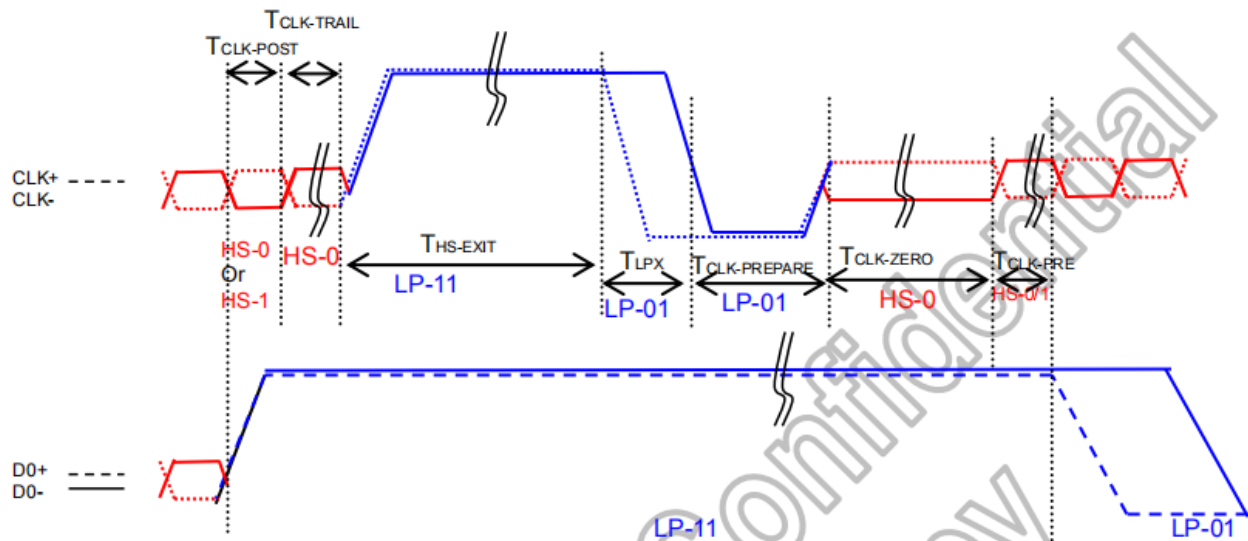
NOTE:

If the last bit is HS-0, the transmitter changes from HS-0 to HS-1
If the last bit is HS-0, the transmitter changes from HS-1 to HS-0

Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_D0P/ DSI_D0P	Time-Out at Display Module to Ignore Transition Period of EoT	T _{HS-SKIP}	40	-	55+4xUI	ns
	Time to Driver LP-11 after HS Burst	T _{HS-EXIT}	100	-	-	ns

*DSI Low Power Mode to High Speed Mode Timing

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Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_CP/ DSI_CN	Time that the MCU shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode	$T_{CLK-POST}$	$60+52xUI$	-	-	ns
	Time to drive HS differential state after last payload clock bit of a HS transmission burst	$T_{CLK-TRAIL}$	60	-	-	ns
	Time to drive LP-11 after HS burst	$T_{HS-EXIT}$	100	-	-	ns
	Time to drive LP-00 to prepare for HS transmission	$T_{CLK-PREPARE}$	38	-	95	ns
	Time-out at Clock Lane Display Module to enable HS Termination	$T_{CLK-TERM-EN}$	-	-	38	ns
	Minimum lead HS-0 drive period before starting Clock	$T_{CLK-PREPARE} + T_{CLK-ZERO}$	300	-	-	ns
	Time that the HS clock shall be driven prior to any associated data Lane beginning the transition from LP to HS mode	$T_{CLK-PRE}$	$8xUI$			

***Clock Lanes High Speed Mode to/from Low Power Mode Timing**

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6.2 Reset timing

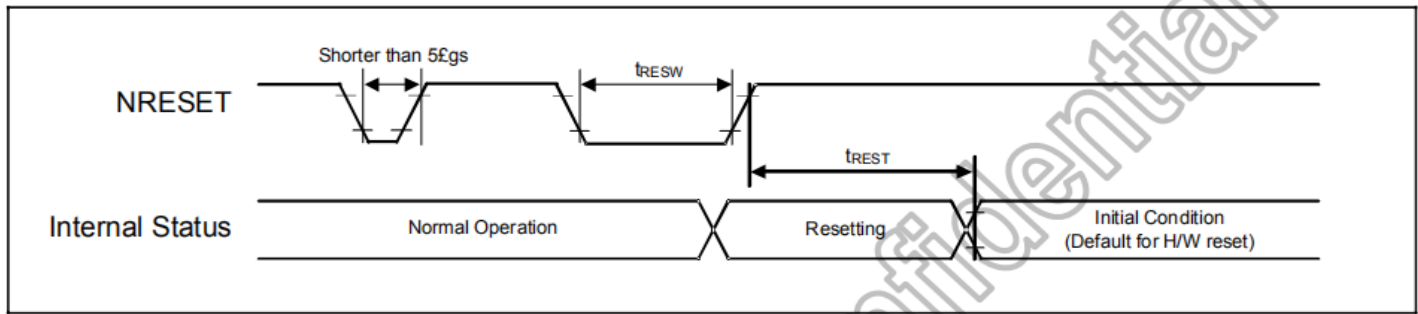


Figure 7.8: Reset input timing

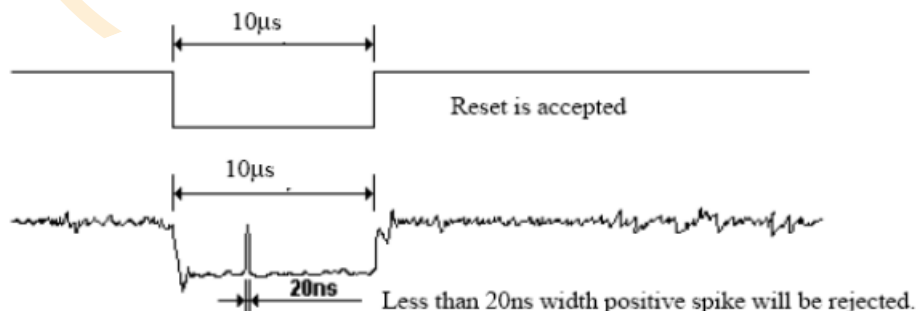
Symbol	Parameter	Related Pins	Spec.			Note	Unit
			Min.	Typ.	Max.		
tRESW	Reset low pulse width ⁽¹⁾	NRESET	10	-	-	-	µs
tREST	Reset complete time ⁽²⁾	-	15	-	-	When reset applied during SLPIN mode	ms
		-	120	-	-	When reset applied during SLPOUT mode	ms

Table 7.8: Reset Input Timing

Note: (1) Spike due to an electrostatic discharge on NRESET line does not cause irregular system reset according to the following table.

NRESET Pulse	Action
Shorter than 5 µs	Reset Rejected
Longer than 10 µs	Reset
Between 5 µs and 10 µs	Reset Start

- (2) During the resetting period, the display will be blanked (The display is entering blanking sequence, which Maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then return to Default condition for H/W reset.
- (3) During Reset Complete Time, ID and VCOM value in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 15ms after a rising edge of NRESET.
- (4) Spike Rejection also applies during a valid reset pulse as shown as below:



- (5) It is necessary to wait 15msec after releasing NRESET before sending commands. Also Sleep Out command cannot be sent for 120msec.

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7. LCD Module Out-Going Quality Level

7.1 VISUAL & FUNCTION INSPECTION STANDARD

7.1.1 Inspection conditions

Inspection performed under the following conditions is recommended.

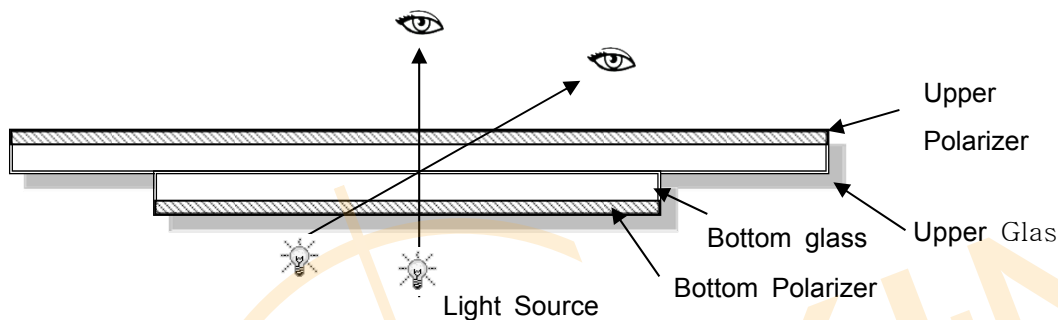
Temperature : $25\pm 5^{\circ}\text{C}$

Humidity : $65\%\pm 10\%\text{RH}$

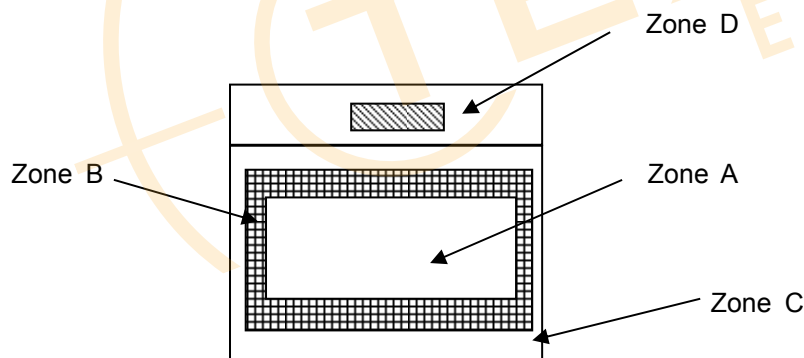
Viewing Angle : Normal viewing Angle.

Illumination: Single fluorescent lamp (300 to 700Lux)

Viewing distance:30-50cm



7.1.2 Definition



Zone A : Effective Viewing Area(Character or Digit can be seen)

Zone B : Viewing Area except Zone A

Zone C : Outside (Zone A+Zone B) which can not be seen after assembly by customer

Zone D : IC Bonding Area

Note:As a general rule ,visual defects in Zone C can be ignored when it doesn't effect product function or appearance after assembly by customer

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7.1.3 Sampling Plan

According to GB/T 2828-2003 ; , normal inspection, Class II

AQL:

Major defect	Minor defect
0.65	1.5

LCD: Liquid Crystal Display , LCM: Liquid Crystal Module,

No	Items to be inspected	Criteria	Classification of defects
1	Functional defects	1) No display, Open or miss line 2) Display abnormally, Short 3) Backlight no lighting, abnormal lighting. etc...	Major
2	Missing	Missing components and etc...	
3	Outline dimension	Overall outline dimension beyond the drawing is not allowed, deformation and etc...	
4	Color tone	Color unevenness, refer to limited sample	Minor
5	Spot/Line defect	Light dot, Dim spot, (Note1) Polarizer Air Bubble, Polarizer accidented spot and etc.	
6	Soldering appearance	Good soldering , Peeling off is not allowed and etc.	
7	LCD/Polarizer	Black/White spot/line, scratch, crack, etc.	

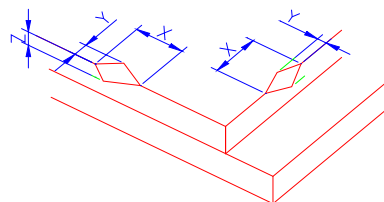
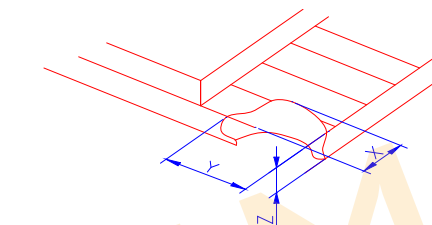
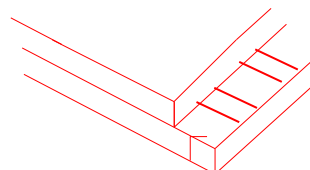
Note1: a) Light dot: Dots appear bright and unchanged in size in which LCD panel is displaying under black pattern.

b) Dim dot: Dots appear dark and unchanged in size in which LCD panel is displaying under pure red, green, blue picture.

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7.1.4 Criteria (Visual)

Number	Items	Criteria(mm)						
1.0 LCD Crack/Broken NOTE: X: Length Y: Width Z: Height L: Length of IT O, T: Height of LCD	(1) The edge of LCD broken	 <table><tr><td>X</td><td>Y</td><td>Z</td></tr><tr><td>≤3.0mm</td><td><Inner border line of the seal</td><td>≤T</td></tr></table>	X	Y	Z	≤3.0mm	<Inner border line of the seal	≤T
	X	Y	Z					
	≤3.0mm	<Inner border line of the seal	≤T					
(2)LCD corner broken	 <table><tr><td>X</td><td>Y</td><td>Z</td></tr><tr><td>≤3.0mm</td><td>≤L</td><td>≤T</td></tr></table>	X	Y	Z	≤3.0mm	≤L	≤T	
X	Y	Z						
≤3.0mm	≤L	≤T						
(3) LCD crack	 Crack Not allowed							



Spot defect

2.0

Y

X

$\Phi=(X+Y)/2$

① light dot (black/white spot , pinhole, stain, etc.)

Zone Size (mm)	Acceptable Qty		
	A	B	C
$\Phi \leq 0.15$	Ignore	Ignore	
$0.15 < \Phi \leq 0.25$	3(distance $\geq 10\text{mm}$)		
$0.25 < \Phi \leq 0.4$	2(distance $\geq 10\text{mm}$)		
$\Phi > 0.4$	0		

② Dim spot (light leakage、dent、dark spot, etc)

Zone Size (mm)	Acceptable Qty		
	A	B	C
$\Phi \leq 0.15$	Ignore	Ignore	
$0.15 < \Phi \leq 0.25$	3(distance $\geq 10\text{mm}$)		
$0.25 < \Phi \leq 0.4$	2(distance $\geq 10\text{mm}$)		
$\Phi > 0.4$	0		

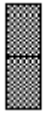
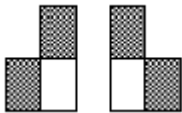
③ Polarizer accidented spot

Zone Size (mm)	Acceptable Qty		
	A	B	C
$\Phi \leq 0.2$	Ignore		Ignore
$0.2 < \Phi \leq 0.5$	2(distance $\geq 10\text{mm}$)		
$\Phi > 0.5$	0		

④Polarizer Bubble

Zone Size (mm)	Acceptable Qty		
	A	B	C
$\Phi \leq 0.2$	Ignore		Ignore
$0.2 < \Phi \leq 0.4$	3(distance $\geq 10\text{mm}$)		
$\Phi > 0.4$	0		



3.0	LCD Pixel defect	Pixel bad points																							
<table border="1"> <thead> <tr> <th>Item</th><th>Zone A</th><th>Acceptable Qt</th></tr> </thead> <tbody> <tr> <td rowspan="3">Bright dot</td><td>Random</td><td>$N \leq 2$</td></tr> <tr> <td>2 dots adjacent</td><td>$N \leq 0$</td></tr> <tr> <td>3 dots adjacent</td><td>$N \leq 0$</td></tr> <tr> <td rowspan="3">Dark dot</td><td>Random</td><td>$N \leq 2$</td></tr> <tr> <td>2 dots adjacent</td><td>$N \leq 0$</td></tr> <tr> <td>3 dots adjacent</td><td>$N \leq 0$</td></tr> <tr> <td>Distance</td><td> 1. Minimum Distance Between Bright dots. 2. Minimum Distance Between dark dots 3. Minimum Distance Between dark and bright dot. </td><td>5mm</td></tr> <tr> <td colspan="2">Total bright and dark dot</td><td>$N \leq 4$</td></tr> </tbody> </table>			Item	Zone A	Acceptable Qt	Bright dot	Random	$N \leq 2$	2 dots adjacent	$N \leq 0$	3 dots adjacent	$N \leq 0$	Dark dot	Random	$N \leq 2$	2 dots adjacent	$N \leq 0$	3 dots adjacent	$N \leq 0$	Distance	1. Minimum Distance Between Bright dots. 2. Minimum Distance Between dark dots 3. Minimum Distance Between dark and bright dot.	5mm	Total bright and dark dot		$N \leq 4$
Item	Zone A	Acceptable Qt																							
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	2 dots adjacent	$N \leq 0$																							
	3 dots adjacent	$N \leq 0$																							
Dark dot	Random	$N \leq 2$																							
	2 dots adjacent	$N \leq 0$																							
	3 dots adjacent	$N \leq 0$																							
Distance	1. Minimum Distance Between Bright dots. 2. Minimum Distance Between dark dots 3. Minimum Distance Between dark and bright dot.	5mm																							
Total bright and dark dot		$N \leq 4$																							
Note: A) Bright dot: Dots appear bright and unchanged in size in which LCD panel is displaying under black pattern. B) Dark dot: Dots appear dark and unchanged in size in which LCD panel is displaying under pure red, green, blue picture. C) 2 dot adjacent = 1 pair = 2 dots Picture:  2 dot adjacent  2 dot adjacent (vertical)  2 dot adjacent  2 dot adjacent (slant)																									



4.0	Line defect (LCD /Polarizer backlight black/white line, scratch, stain)				
					
	W: width, L : length				
	N : Count				

Criteria (functional items)

Number	Items	Criteria (mm)
1	No display	Not allowed
2	Missing segment	Not allowed
3	Short	Not allowed
4	Backlight no lighting	Not allowed

8. Reliability Test Result

Item	Condition	Inspection after test
High Temperature Operating	85°C,96H	Inspection after 2~4hours storage at room temperature, the sample shall be free from defects: 1.Air bubble in the LCD; 2.Non-display; 3.Missing segments/line; 4.Glass crack; 5.Current IDD is twice higher than initial value.
Low Temperature Operating	-30°C, 96HR	
High Temperature Storage	85°C, 96HR	
Low Temperature Storage	-30°C, 96HR	
High Temperature & High Humidity Operating	+60°C, 90% RH ,96 hours.	
Thermal Shock (Non-operation)	-30°C,30 min ↔ +80°C,30 min, Change time:5min 20CYC.	
ESD test	C=150pF, R=330,5points/panel Air:±8KV, 5times; Contact:±6KV, 5 times; (Environment: 15°C~35°C, 30%~60%).	
Vibration (Non-operation)	Frequency range:10~55Hz, Stroke:1.5mm Sweep:10Hz~55Hz~10Hz 2 hours for each direction of X.Y.Z. (6 hours for total) (Package condition).	
Box Drop Test	1 Corner 3 Edges 6 faces,80cm(MEDIUM BOX)	

Remark:

- 1.The test samples should be applied to only one test item.
- 2.Sample size for each test item is 5~10pcs.
- 3.For Damp Proof Test, Pure water(Resistance > 10MΩ) should be used.
- 4.In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judged as a good part.
- 5.Failure Judgment Criterion: Basic Specification, Electrical Characteristic, Mechanical Characteristic, Optical Characteristic.
6. The color fading mura of polarizing filter should not care.

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9. Cautions and Handling Precautions

9.1 Handling and Operating the Module

(1) When the module is assembled, it should be attached to the system firmly.

Do not warp or twist the module during assembly work.

(2) Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.

(3) Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.

(4) Do not allow drops of water or chemicals to remain on the display surface.

If you have the droplets for a long time, staining and discoloration may occur.

(5) If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.

(6) The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane.

Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.

(7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.

(8) Protect the module from static; it may cause damage to the CMOS ICs.

(9) Use finger-stalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.

(10) Do not disassemble the module.

(11) Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.

(12) Pins of I/F connector shall not be touched directly with bare hands.

(13) Do not connect, disconnect the module in the "Power ON" condition.

(14) Power supply should always be turned on/off by the item 6.1 Power On Sequence & 6.2 Power Off Sequence

9.2 Storage and Transportation.

(1) Do not leave the panel in high temperature, and high humidity for a long time.

It is highly recommended to store the module with temperature from 0 to 35 °C and relative humidity of less than 70%

(2) Do not store the TFT-LCD module in direct sunlight.

(3) The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.

(4) It is recommended that the modules should be stored under a condition where no condensation is allowed. Formation of dewdrops may cause an abnormal operation or a failure of the module.

In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.

(5) This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.

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10. Packing

TBD



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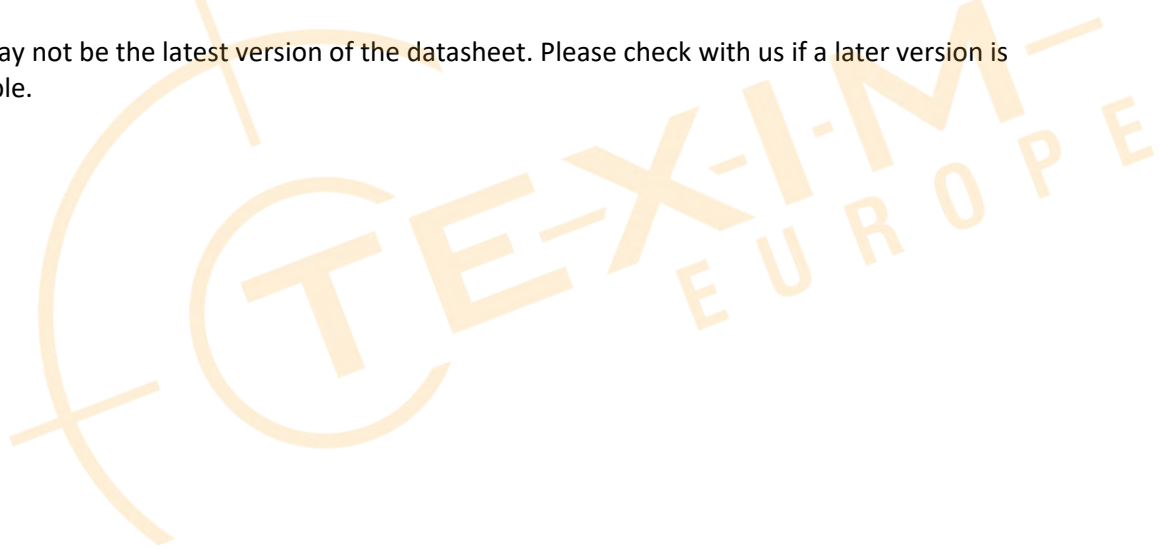
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